REMARKS

Claims 1-12 and 22 were pending in the application. Claim 24 has been added. Accordingly, claims 1-12, 22, and 24 are now pending in the application.

Allowable Subject Matter

Claims 3-10 were objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claims and any intervening claims. Applicant appreciates Examiner's consideration of these claims.

35 U.S.C. § 103 Rejections

1. Claims 11-12 were rejected under 35 U.S.C. §103(a) as being unpatentable over Smith et al. (U.S. Publication No. 2004/0162697). Applicant respectfully traverses this rejection.

Applicant respectfully submits that Smith fails to teach or suggest "selectively inserting one or more idle clock cycles between a first memory access and a second memory access depending upon said sensed temperature" as recited by claim 11.

The Examiner contends that paragraph [0047] of Smith teaches the above-highlighted features of claim 11. Applicant respectfully disagrees. Smith teaches, in paragraph [0047]:

> "Self-monitoring may be extended to implement cooling logic 43 as a matter of design choice. If cooling logic 43 is not implemented, the digital output from step 38 may be used to signal another apparatus of a threshold temperature comparison result. If cooling logic 43 is implemented, test 44 determines if there is an over-temperature condition. Test 48 determines if a cooling action is already active. If so, the cooling action is continued. If a cooling action is not active, then a cooling action is activated 52. As a matter of design choice, test 44 may make a single comparison, wherein a single cooling action may be initiate 52 (e.g., turn on the fan when an over-temperature condition is detected) or test 44 may test the digital signal against a multitude of thresholds, wherein a plurality of cooling actions may be initiated 52 (e.g., activate a fan, slow the clock speed, operator notification, system shut-down). If test 44 determines there is no over-temperature

condition, then test 46 determines if a cooling action is active 46, and if so discontinues 50 a cooling action. As an implementation option, a second "shut-off" temperature may be implemented for each corresponding cooling action "turn-on" temperature. Discontinuing 50 of a cooling action may be conditional on an additional test determining if the cooling action initiated 52 is below the "shut-off" temperature and therefore redundant before discontinuing 50 a cooling action. If test 46 determines there is no cooling action active, processing continues. Delay 54, which may be of zero or more clock cycles or event triggered, idles process 30 when **additional readings are not required**. After delay 54 processing continues with application 32 of a voltage to the thermal diode". (Emphasis added)

Smith teaches that when additional temperature readings are not required, delay 54 idles a re-start of process 30 by one or more clock cycles. In Smith, a second iteration of process 30 is delayed until a subsequent temperature reading is required. However, Smith fails to teach or suggest "selectively inserting one or more idle clock cycles between a first memory access and a second memory access **depending upon said sensed temperature**" as recited by claim 11. Accordingly, claim 11 is believed to patentably distinguish over Smith. Claim 12 is dependent upon claim 11 and is therefore believed to patentably distinguish over Smith for at least the same reasons.

Additionally, Smith fails to teach or suggest "wherein in response to said sensed temperature being greater than a predetermined threshold, inserting said one or more idle clock cycles between a plurality of memory accesses at a particular rate" as recited in claim 12. In accordance, claim 12 is believed to patentably distinguish over Smith.

2. Claims 1-2, 11-12, and 22 were rejected under 35 U.S.C. 103(a) as being unpatentable over Soltis, Jr. et al. (U.S. Publication No. 2004/0117678). Applicant respectfully traverses this rejection.

Applicant respectfully submits that Soltis fails to teach or suggest "wherein said memory controller is configured to selectively insert one or more idle clock cycles between a first memory access and a second memory access depending upon said sensed temperature" as recited by claim 1.

The Examiner contends that paragraph [0038] of Soltis teaches the above-highlighted features of claim 1. Applicant respectfully disagrees. Soltis teaches, in paragraph [0038]:

> "Since the low performance operating point has longer access time than the high performance operating point, this operating point requires additional latency delay clock cycles **if** it is to be used with a high performance operating point of the processor. In a particular embodiment, the higher-level cache memory 120 is therefore designed with a programmable latency. In a particular embodiment the latency allocable to **cache memory access** is programmable to a number of clock cycles between two and six". (Emphasis added)

While Soltis teaches adjusting cache latency, Soltis fails to teach or suggest "wherein said memory controller is configured to selectively insert one or more idle clock cycles between a first memory access and a second memory access depending upon said sensed temperature" as recited by claim 1. In accordance, claim 1 is believed to patentably distinguish over Soltis. Claim 2 is dependent upon claim 1 and is therefore believed to patentably distinguish over Soltis for at least the same reasons.

Likewise, claims 11 and 22 recite features similar to those highlighted above with respect to independent claim 1. Specifically, claim 11 recites "selectively inserting one or more idle clock cycles between a first memory access and a second memory access depending upon said sensed temperature", and claim 22 recites "a service processor coupled to said memory controller, wherein in response to said sensed temperature being greater than a predetermined threshold, said service processor is configured to program said memory controller to insert one or more idle clock cycles between a first memory access and a second memory access". Claims 11 and 22 are therefore believed to patentably distinguish over Soltis for at least the reasons given in the above paragraphs discussing claim 1. Claim 12 depends on claim 11 and is therefore believed to patentably distinguish over Soltis for at least the same reasons.

Furthermore, Applicant requests examination of added claim 24. Applicant respectfully submits that Soltis fails to teach or suggest "wherein said service processor is configured to change a number of idle cycles that are inserted between a plurality of additional memory

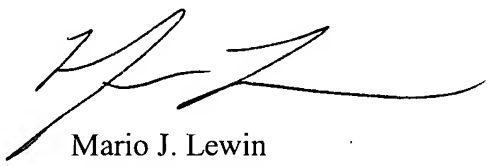
accesses depending upon said sensed temperature" as recited by claim 24. In accordance, claim 24 is believed to patentably distinguish over Soltis.

CONCLUSION

In light of the foregoing amendments and remarks, Applicant submits that all pending claims are in condition for allowance, and an early notice to that effect is earnestly solicited. If a phone interview would speed allowance of any pending claims, such is requested at the Examiner's convenience.

If any extensions of time (under 37 C.F.R. § 1.136) are necessary to prevent the above referenced application(s) from becoming abandoned, Applicant(s) hereby petition for such extensions. If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5681-73900/BNK.

Respectfully submitted,



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